

Appl. No. 10/061,384
Amdt. dated June 14, 2005
Reply to Office Action of January 14, 2005

Amendments to the Drawings:

The attached sheet of drawings includes changes to FIG.4.
This sheet, which includes FIG.4, replaces the original sheet
including FIG.4.

Attachment: Replacement Sheet

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REMARKS

Claims 1 to 27 were pending in the application at the time of examination. The Examiner objected to Applicants' FIG.4. The Examiner rejected Claims 1 to 27 under 35 U.S.C. 103(a) as obvious over the Hobbs et al reference (2002/01991178 A1).

Applicants have amended FIG.4 as shown in the replacement sheet for FIG.4 filed herewith. Claims 1 to 27 remain in the application.

OBJECTION TO FIG.4

The Examiner objected to Applicants' FIG.4.

Applicants have amended FIG.4 as shown in the replacement sheet for FIG.4 filed herewith. In light of the amendment to FIG.4, Applicants' respectfully request the Examiner withdraw the objections to FIG.4.

REJECTION OF CLAIMS 1 TO 27

The Examiner objected to Applicants' FIG.4. The Examiner rejected Claims 1 to 27 under 35 U.S.C. 103(a) as obvious over the Hobbs et al reference (2002/01991178 A1).

Applicants' independent Claim 1 reads as follows, with emphasis added:

A method of optimizing instructions included in a program being executed, the method comprising:
collecting information describing a frequency of occurrence of a plurality of cache misses caused by at least one instruction;

identifying a performance degrading instruction;
optimizing the program to provide an optimized sequence of instructions, the optimized sequence of instructions comprising at least one prefetch instruction; and

modifying the program being executed to include the optimized sequence.

Applicants' independent Claim 13 reads as follows, with emphasis added:

A method of optimizing a program comprising a plurality of execution paths, the method comprising:
collecting information describing a plurality of occurrences of a plurality of cache miss events during a runtime mode of the program;
identifying a performance degrading execution path in the program;
modifying the performance degrading execution path to define an optimized execution path, the optimized execution path comprising at least one prefetch instruction;
storing the optimized execution path; and
redirecting the performance degrading execution path in the program to include the optimized execution path.

Applicants' independent Claim 26 reads as follows, with emphasis added:

A computer-readable medium having a computer program accessible therefrom, wherein the computer program comprises instructions for:
collecting information describing a frequency of occurrence of a plurality of cache misses caused by at least one instruction;
identifying a performance degrading instruction;
optimizing the computer program to provide an optimized sequence of instructions, the optimized sequence of instructions comprising at least one prefetch instruction; and
modifying the computer program being executed to include the optimized sequence.

Applicants' independent Claim 27 reads as follows, with emphasis added:

A computer system comprising:
a processor;
a memory coupled to the processor;
a program comprising instructions, the program being stored in memory, the processor executing instructions to:
collect information describing a frequency of occurrence of a plurality of cache misses caused by at least one instruction;
identify a performance degrading instruction;
optimize the program to provide an optimized sequence of instructions, the optimized sequence of instructions comprising at least one prefetch instruction; and
modify the program being executed to include the optimized sequence.

As shown above each of Applicants' independent Claims 1, 13, 26 and 27 specifically recite collecting information describing a frequency of occurrence of a plurality of cache misses, or words to that effect.

Applicants respectfully submit that the Examiner has failed to show where in the Hobbs reference it is disclosed, taught or suggested collecting information describing a frequency of occurrence of a plurality of cache misses as recited in Applicants' Claims 1, 13, 26 and 27.

In addition, Applicants' independent Claim 25 reads as follows, with emphasis added:

A method of optimizing a program, the method comprising:
receiving information describing a dependency graph for an instruction causing frequent cache

misses, the instruction being included in the
program;

determining whether a cyclic dependency pattern
exists in the graph;

if the cyclic dependency pattern exists then,
computing stride information derived from the cyclic
dependency pattern;

inserting an at least one prefetch instruction
derived from the stride information, the at least one
prefetch instruction being inserted into the program
prior to the instruction causing the frequent cache
misses;

reusing the at least one prefetch instruction in
the program for reducing subsequent cache misses; and

performing said receiving, said determining,
said computing, said inserting and said reusing
during runtime of the program.

Applicants further respectfully submit that the Examiner
has failed to show where in the Hobbs reference it is
disclosed, taught or suggested:

receiving information describing a dependency
graph for an instruction causing frequent cache
misses, the instruction being included in the
program;

determining whether a cyclic dependency pattern
exists in the graph;

as recited in Applicants' Claim 25.

The Examiner is reminded that:

To establish a *prima facie* case of obviousness, three
basic criteria must be met. First, there must be some
suggestion or motivation, either in the references
themselves or in the knowledge generally available to
one of ordinary skill in the art, to modify the
reference or to combine reference teachings. Second,
there must be a reasonable expectation of success.
Finally, the prior art reference (or references when

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combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (

(MPEP 2142 with emphasis added)

Applicants respectfully submit that the Examiner has failed to show that the prior art reference (Hobbs) teaches or suggests all the claim limitations as discussed above. Consequently, Applicants respectfully request the Examiner withdraw the rejection of Claims 1, 13, 25, 26, and 27 based on Hobbs and 35 U.S.C. 103(a).

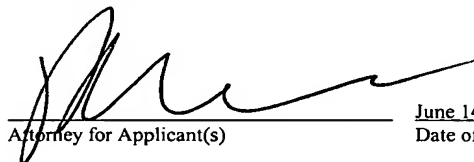
In addition, Claims 2 to 12 depend, directly or indirectly, on Claim 1 and Claims 14 to 24 depend, directly or indirectly, on Claim 13. Therefore Applicants respectfully request the Examiner withdraw the rejection of Claims 2 to 12 and 14 to 24 as well.

CONCLUSION

For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicants.

CERTIFICATE OF MAILING


I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 14, 2005.



Attorney for Applicant(s)

June 14, 2005
Date of Signature

Respectfully submitted,


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